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AN10658

Sending I²C-bus signals via long communications cables

Rev. 01 — 26 February 2008 Application note

Document information

Info	Content
Keywords	I2C-bus, twisted pair cables, Cat5e, high speed, Fast-mode, Fast-mode Plus, Fm+, inter-IC, SDA, SCL, P82B96, PCA9600, I2C2005-1
Abstract	Reliable I²C-bus communication at high data rates, and over many meters, can be achieved using widely available twisted-pair communication cable (e.g. Category 5e and similar 4-pair cables, as typically used for Ethernet communications). The two bidirectional I²C-bus signals, SDA and SCL, are split into four unidirectional signals using P82B96 or PCA9600. Each signal is then transmitted over a separate twisted pair within the communication cable and combined again by another P82B96. The configuration minimizes cable propagation delays and therefore maximizes speed because transmission line reflections do not affect the signal integrity. Differences in local ground potential between the cable ends of at least 5 V (of either polarity, or ac peak) will not affect the data integrity. High levels of ESD immunity can be achieved when required. I²C-bus maximum clock speed calculator.

Revision history

Rev	Date	Description
01	20080226	Application note; initial version

Contact information

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1. Introduction

This document discusses the timing and signal integrity requirements to achieve reliable communications at relatively high speeds (at least 400 kHz) when it is required to send I²C-bus signals over relatively long distances (at least 100 m at lower speeds) using conventional communications cables. The cables chosen are known as Category 5e communication cables and contain four twisted pairs having a characteristic impedance around 100 Ω.

The drive capability of standard I²C-bus devices (3 mA sink) or even of Fast-mode Plus (Fm+) or I²C-bus buffers such as P82B96 or PCA9600 (30 mA) is not sufficient to drive useful logic voltages on these cables if they are terminated by their characteristic impedance at each end. Working with termination resistances that must be significantly larger than the characteristic impedance of the cable means there will be significant distortion of the logic signals in the period immediately following a change in the required logic state.

When there are large distances between the ends of the connecting cable some differences in the local ground potentials can be expected and need to be considered.

The 4-wire driving method shown in Figure 2 minimizes the signal distortions and guarantees each logic transition can be transmitted in the minimum possible time—the simple one-way propagation delay of the cable.

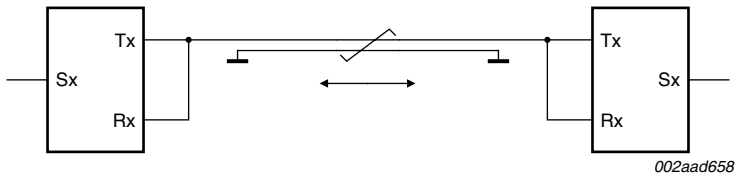


Fig 1. Conventional bidirectional signal transmission over a twisted pair cable

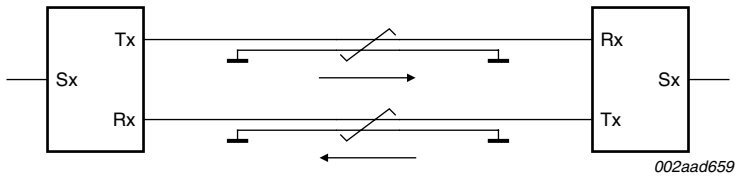


Fig 2. Split signal transmission using two twisted pairs and unidirectional signals

Figure 1 and Figure 2 show the two possible ways that P82B96 or PCA9600 can be configured to send, for example, the SCL signal when driving twisted pairs. The pull-up resistors are **not** shown, but their possible position and values are discussed in this note. Ty/Ry/Sy will use the same configurations to send the SDA signal.

A daughter card to fit the I2C2005-1 Evaluation board and demonstrate the special signaling is described. Switch options also allow it to be configured as in Figure 1 to produce Fm+ compliant signals.

1.1 Typical speed performance that can be achieved

The typical speed performance that can be achieved are:

Example A: 2 × PCA9600 communicating at 800 kHz over 20 m of Cat5e cable and exchanging 800 kHz, 3 mA level, I²C-bus signals with an Fm+ capable slave.

Example B: 2 × P82B96 communicating at 400 kHz over 50 m of Cat5e twisted pair cable and exchanging 400 kHz Fast-mode I²C-bus compatible signals (i.e., 3 mA levels) with an Fm+ capable slave.

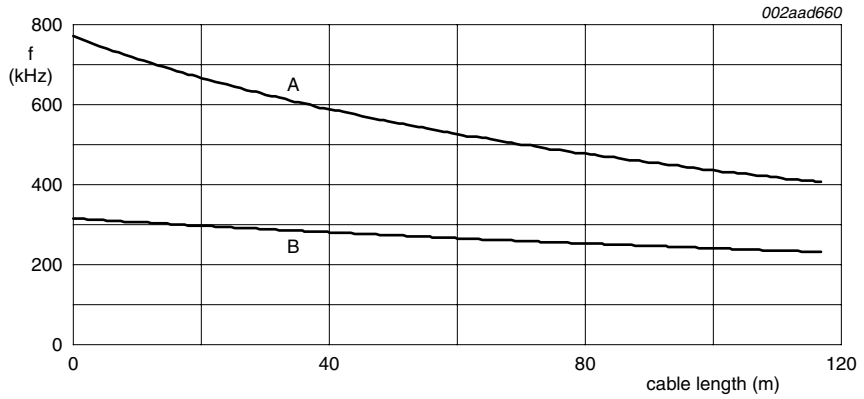
Example C: 1 × P82B96 converting 3 mA I²C-bus levels to 30 mA levels and directly interfacing with an Fm+ slave at > 700 kHz.

Example D: 1 × PCA9600 converting 3 mA Fm+ I²C-bus signals to 30 mA Fm+ signals and directly interfacing with an Fm+ slave at 1 MHz.

(In Example B, directly replacing P82B96 by PCA9600 would achieve the same 50 m performance with slightly improved timing margins, but more importantly, PCA9600 provides guaranteed TTL level compatibility at its Sx/Sy while P82B96 is only typically compatible with TTL logic levels.)

Figure 3 shows the theoretical speed limitation for the 4-signal mode, based on assuming that all components have the worst case timing performance for their class. The curve is calculated by simply adding the total system propagation delays to the allowed minimum low clock period.

As shown in the examples, when the connected parts have their typical delays, or if Fm+ parts are used in a Fast-mode system, then the speeds can be significantly higher. Cables longer than 100 m are of course possible, but the limitation with 5 V logic levels can become factors other than just propagation delays, for example attenuation due to cable losses.



A = Fm+ capable parts with PCA9600

B = Fast-mode capable parts with P82B96

Fig 3. Theoretical speed performance using 4-signal mode

1.2 Improved immunity to ESD, noise, and ground potential differences

Because the cable is low-impedance it is possible to fit transient protection devices having relatively large capacitance without significantly disturbing the logic signals. That enables a system to be designed with high tolerance to ESD.

When there are long cable runs there can be significant differences in the local equipment 'ground' potential at each end of the cable. Generally it will be necessary to connect the logic signal ground wires to the local ground at each piece of connected equipment and this has the potential to cause currents in the ground wires and level shifting of the logic signals at the send/receive ICs. These shifts in level reduce the noise margins of the logic signals, i.e., they reduce the margin between the actual logic voltage level and the level that will cause the signal to be recognized as the opposite logic state.

The levels shifts can also cause the voltages applied to the I/Os of the driving chips to exceed their absolute maximum ratings. An important case is the application of voltages that are negative with respect to the chip's ground pin. The usual limit is around −0.5 V and that will generally limit the difference in ground potentials to 0.5 V.

With the arrangement described it is possible to build a system that can tolerate ground differences of at least 5 V (either polarity or peak ac value).

2. The benefits of extending an I²C-bus

The I²C-bus is already widely used within each separate unit of many pieces of equipment, for example in consumer electronics in TV, DVD, and STB or in the modules or racks of telecommunications and industrial electronics.

It makes sense to 'extend' the use of the I²C-bus to the linking of those pieces of equipment rather than converting the I²C-bus signals to use some unrelated data transmission system.

The ability to use a conventional communications cable and its associated low cost hardware to make a robust control link between pieces of equipment makes this option even more attractive.

3. Using the P82B96/PCA9600 board with the I2C2005-1 evaluation board

The schematic for the P82B96/PCA9600 evaluation board is shown in Figure 4.

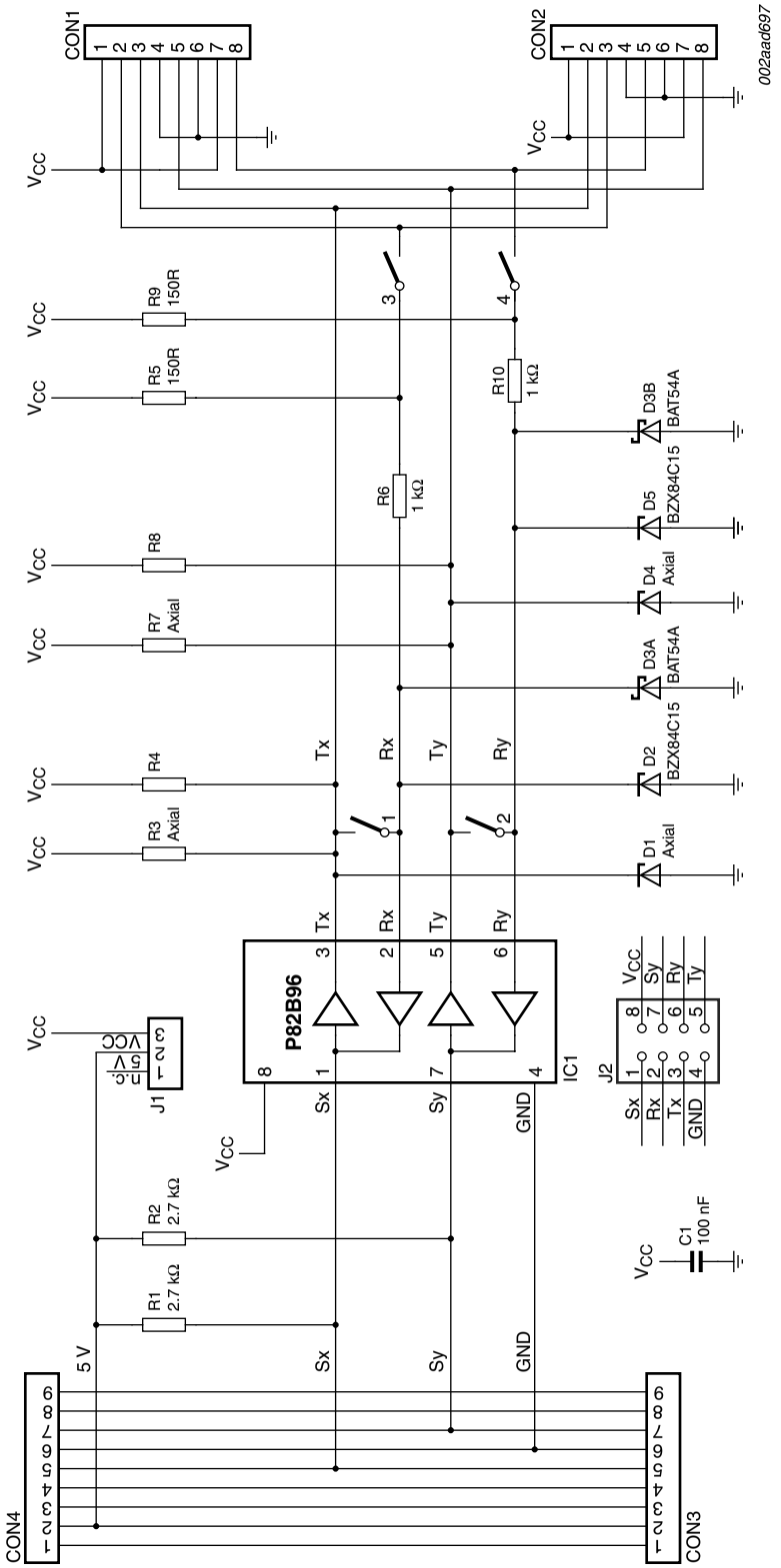


Fig 4. Schematic of P82B96/PCA9600 evaluation daughter card for I2C2005-1 evaluation board

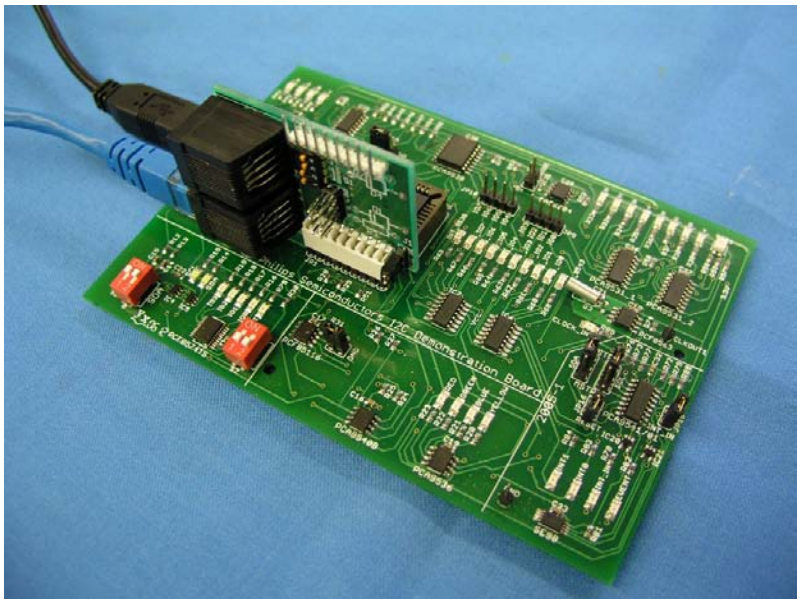


Fig 5. P82B96/PCA9600 daughter board fitted to the 9-pin header on I2C2005-1

This daughter board can be configured to demonstrate two different applications:

- Generating an Fm+ compatible drive signal for other application boards

  A single daughter board is fitted to the 9-pin expansion header of the I2C2005-1 evaluation board and can be powered from the switched 5 V supply on that board.

  The I2C2005-1 evaluation board's 9-pin header signals are duplicated on the daughter board's 9-pin header CON4 to allow further expansion or connection of other daughter cards.

  The P82B96/PCA9600 generates Fm+ signals on the 8P8C modular (RJ45) jack CON1 that are compatible with, for example, the PCA9633 LED Demo Board Fm+ signals.

  To select this option it is necessary to close switches 1 and 2 on the DIP switch S1 and to open switches 3 and 4. (The RJ45 jack CON2 should not be used.)

  The 5 V power selection jumper should be fitted between pins 2 and 3 on header J1.

  The input signals from the I2C2005-1 evaluation board and the corresponding Fm+ signals as delivered to the RJ45 jack CON1 are available for probing on the 8-pin header J2.

  See Section 3.1 for further details of this application.

- Driving long Cat5e communication cables in '4-signal' mode using two daughter boards

  One board is fitted to the 9-pin expansion header of the I2C2005-1 evaluation board and can be powered from the switched 5 V supply of that board by fitting the jumper between pins 2 and 3 on header J1.

  The board is configured for driving long Cat5e cables by opening switches 1 and 2 on the DIP switch S1 and closing the switches 3 and 4.

  The cable to be driven, fitted with standard 8P8C modular connectors (RJ45), is fitted into the RJ45 jack CON1.

The other end of the cable is fitted into the RJ45 jack CON2 of a second or 'remote' P82B96/PCA9600 daughter board. This 'remote' board will derive its 5 V supply from the first board, via the cable and CON2. Use of CON2, with its different wiring configuration, provides the necessary crossover linking from Tx on one board to Rx on the other.

Ensure that the 5 V power selection jumper is fitted between pins 2 and 3 on header J1 or that some alternative logic supply voltage is connected to pin 2 on J1 so that there is a supply voltage for the I²C-bus on the Sx/Sy side of this 'remote' board.

The cable bus signals will be converted back to conventional I²C-bus levels by the 'remote' P82B96/PCA9600 and both the cable bus and I²C-bus signals are available for probing on the 8-pin header J2. They are also available on the 9-pin header CON4 in the same format as on the I2C2005-1 expansion header.

Note that only the 'switched 5 V' supply from the I2C2005-1 board is used on CON1/CON2. The un-switched 5 V and 3.3 V supplies are not available on the Cat5e cable and therefore are not available on CON4 in modes where boards are linked only by the Cat5e cable.

See Section 3.2 for further details of this application.

3.1 Generating Fm+ compatible signals at CON1

This operating mode is intended for providing Fm+ drive signals to enable testing of ICs or modules that require up to 30 mA driver sink capability to allow low resistance pull-ups to be used to achieve fast rise times.

The pull-up resistor actually fitted on the P82B96/PCA9600 demonstration board is 1.15 kΩ, being the series combinations of R5 + R6 and R9 + R10.

Provision is made for fitting either leaded or chip resistors in parallel with this pull-up to achieve whatever resultant value is desired. Those resistors may be fitted as R4,5,8,9.

Note that to meet the 120 ns Fm+ rise time requirement the maximum capacitance load allowed with the fitted 1.15 kΩ pull-up is only 120 pF. The typical blue Cat5e communication cable is about 46 pF/m so connection cables must be kept short.

It is recommended **not** to attempt driving long cables with this pull-up value; the 4-signal mode is much more reliable and allows higher speed.

An example of using the board in this Fm+ mode would be to directly drive the FDI PCA9633 LED driver demonstration board's Fm+ bus using a short communications cable between CON1 and either RJ45 jack on the FDI board. The settings on the boards should be:

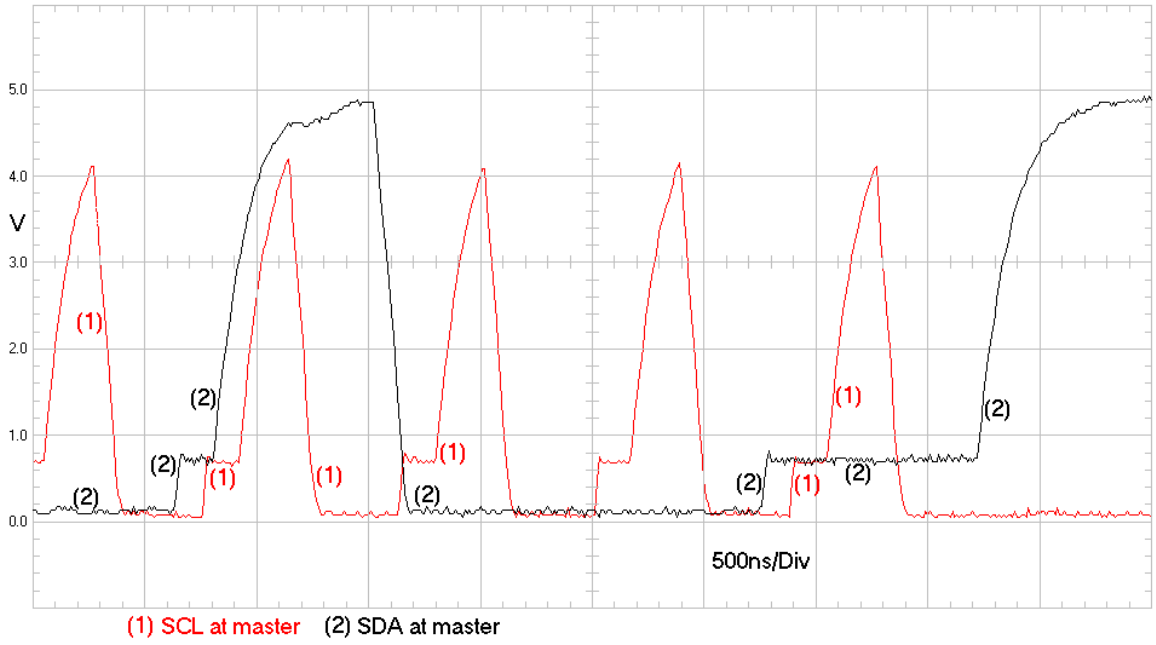
- On the P82B96/PCA9600 daughter board:
  - V_{CC} jumper in place, so the board is powered from the I2C2005-1
  - Switches 1 and 2 closed (on) [Selects Fm+ mode]
  - Switches 3 and 4 open (off) [Selects Fm+ mode]
- On the FDI PCA9633 demo board:
  - Switches 1-3 set as advised in the 2005-1 user guide [address selection]. The address used with Win USB Lite requires Switch 1 = ON, Sw 2 = OFF, Sw 3 = ON.
  - Switch 4 ON. [The cable core 6 is used as a ground and this sets OE low = active.]

- Switch 5 and 6 ON. [Parallels the 1 kΩ pull-ups onto the cable for faster rise time]
- Switch 7 OFF. [Limited current available from I2C2005-1 board, so disable cable supply]
- Battery in place, and switch 8 ON. [Powers the PCA9633 board from the 9 V battery, or from some other power source that must be provided by the user. While it might also be possible to close switch 7 and open switch 8 so the application is powered via the cable from the I2C2005-1 board and its USB supply, the total current drawn by LEDs, pull-ups, etc., is variable and must be checked by any user wanting to try this mode]

With the advised settings the resultant pull-up on the Fm+ bus on the cable is 1 kΩ in parallel with 1.15 kΩ, so 535 Ω. The bus speed will be limited by the rise time of this cable bus as well as by the propagation delays of the buffer.

With a short cable, say 2 m, the clock speed may be selected as 1 MHz on the USB Lite interface screen, and communications will be fine, but the true speed will be lower than the displayed value due to clock stretching by the buffer. For example when using P82B96 the actual clock rate will be measured at about 725 kHz. For 100 kHz operation, the 1 μs rise time limit will be reached when the cable length is about 50 m. For 400 kHz, the 300 ns rise time limit will be reached with just 14 m of cable but those timings are only the specification requirements and typical operation at higher frequencies will be found possible.

If short cables are used (≤ 1 m) and stronger pull-ups are fitted at the Sx/Sy pins then Fm+ operation to a true 1 MHz should be obtained with PCA9600 when the slave devices are Fm+ capable. To observe the limit when using the I2C2005-1 board and software it is necessary to add parallel 4.7 kΩ resistors at Sx/Sy on the daughter board fitted to the I2C2005-1 board and to select an illegal value for I²C-bus frequency. Try entering 1142 kHz. The bus will communicate correctly and the actual clock is 1.142 MHz. The bus data timings have good margins but the SCL HIGH period is less than the Fm+ minimum timing requirement as shown in Figure 6. This master can subtract up to 125 ns from the nominal HIGH period for certain values of the LOW period stretching by the buffer. (This master is only rated to 400 kHz clock.)



Remark: Note that SCL HIGH is less than 200 ns.

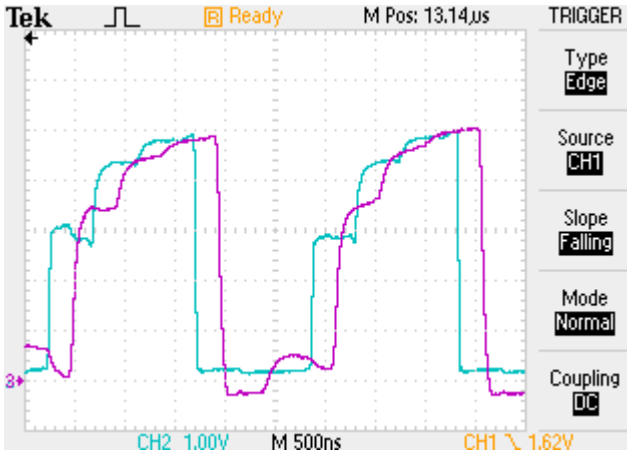
Fig 6. 1.142 MHz Fm+ mode transmission over 2 m

3.2 Driving long Cat5e cables in 4-signal mode

As explained in Section 4.1, this mode achieves the shortest signal propagation times possible, within the drive capability of Fm+ parts, for any given length of cable.

The board mounted on the I2C2005-1 board uses P82B96/PCA9600 to convert the I²C-bus signals from CON3 into unidirectional logic signals. Tx generates the 'send' logic signal on one twisted pair and Rx receives the signals that are generated by Tx on a second board. Note the signals on the four cable cores are no longer I²C-bus signals, so they are not required to conform to I²C-bus rise times or levels. They are designed to match the level requirements of Rx and that has switching levels very close to V_{CC} / 2.

As described in Section 4.1, the 30 mA Tx sink capability allows a bus pull-up of 150 Ω and this is placed at the receiving end of the cable to achieve the fastest rise of that received signal to a level above V_{CC} / 2.



Cyan = Tx sent

Magenta = Rx received

Fig 7. 400 kHz sent and received waveforms on a 46 m cable using P82B96

Typical waveforms on a 46 m cable are shown in Figure 7. The cyan trace shows the 'send' signal generated at Tx. It is pulled LOW to approximately 0.2 V by the strong sink capability of Tx even though the 'dynamic' load is the 100 Ω cable characteristic impedance.

That LOW propagates along the cable and approximately 250 ns later it arrives at the far end of the cable as shown by the falling edge of the magenta trace. The magenta trace is the signal on the Rx pin of the 'receiving' board. Because the cable is not correctly terminated the received signal on the cable will have a large negative component followed by some ringing but the series 1 kΩ and the Schottky diode at Rx limit the negative signal to −0.25 V as shown and the remaining peak positive component of the ringing is less than 0.5 V.

When Tx releases the cable bus it immediately rises to approximately 2.8 V. That level propagates along the cable and when it reaches the remote end of the cable it represents a step level of 2.8 V ahead of the cable impedance (100 Ω). The actual received signal level is modified by the 150 Ω pull-up to 5 V and cable losses but it tends towards a final value of about 3.8 V. The important characteristic is that it crosses the V_{CC} / 2 switching level at Rx only slightly later than the nominal 250 ns cable propagation delay time after the Tx changes.

While the propagation delays on the cable have been minimized by this method the system designer must account for all wiring and IC propagation delays when designing the system. In this configuration, the P82B96/PCA9600 will not cause the more usual clock (or data) stretching at the end of each LOW period because there is no need for the Sx LOW signal to become HIGH throughout the path Sx-Tx-Rx and back to Sx. The characteristic 0.7 V to 1 V 'step' on the rising edges of the signals at Sx pins is absent.

It is possible to use CON3 or CON4 on the second or 'remote' board to pass I²C-bus compatible signals to another application that uses a different logic supply and levels. In this case ensure that different logic supply voltage is connected to pin 2 of CON3 or CON4 and then J1 is left open. The logic levels on CON3/CON4 will match the logic supply provided on pin 2 of the remote board. The pull-up is 2.7 kΩ.

When there is no other logic supply used for the second/remote board the jumper J1 must be closed so the cable supply voltage is connected to the 2.7 kΩ pull-ups on Sx. The waveforms at Sx are then available for probing at J2 and, with 5 V logic levels, at CON3 and CON4.

3.3 Alternative components for ESD protection

As described in Section 4.3, provision is made for fitting of ESD protection components to achieve very high levels of immunity when this is a requirement.

Diodes D1, D4 can be large axial or SMD protection diodes to provide for the Tx pin. They should be chosen to clamp the peak voltage at Tx to the maximum rating (18 V) of this pin when the required test pulses are applied to the cable. Diodes D2, D5 can be smaller SMD Zener diodes from the BZX84-Cxx or similar families.

4. Sending I²C-bus signals over communications cables

4.1 The signaling arrangement and its timing advantage

Figure 8 shows the basic arrangement used to transmit each of the I²C-bus signals, either SCL or SDA.

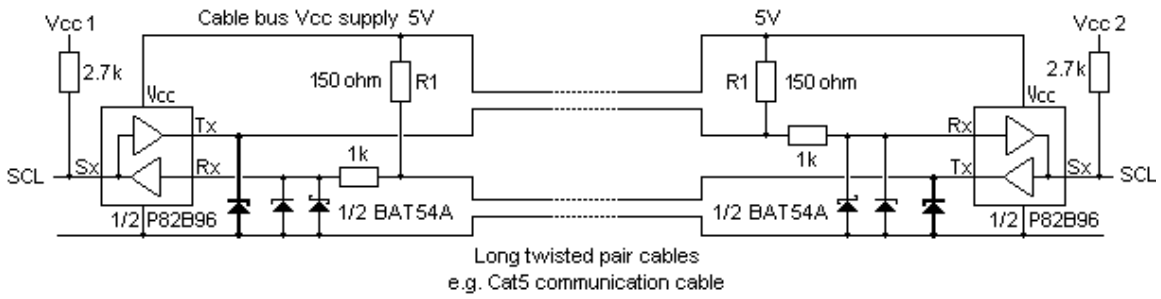


Fig 8. The basic arrangement for one signal, SCL or SDA

P82B96 is used in its conventional way to split the bidirectional I²C-bus signal into two unidirectional components Tx and Rx. Tx is the logic signal to be transmitted over the cable to a remote node and Rx is the logic signal received from that remote node.

Selecting a conventional 5 V supply for the cable signals involves a compromise between speed and noise immunity. For noise immunity a 15 V supply has obvious advantages but then the pull-up resistor, to match the 30 mA static sink capability at Tx, would be 500 Ω and that is then much larger than the characteristic impedance of the cable (100 Ω). The cable signal rise time will be slower than for a lower termination resistance because it will take several reflections on the cable before the logic level settles above the 7.5 V logic switching threshold. For highest speed, a 5 V signaling level is a better compromise.

5 V supply allows a minimum pull-up of 153 Ω and cable resistance, at around 9 Ω/100 m for the sum of the two cores that make each pair, means a nominal 150 Ω pull-up will be fine. (Tx is specified to sink 60 mA at the higher saturation of 1 V, so it is not necessary to have 1 mA accuracy in the sink current value).

The bus pull-up has been placed as a single resistor at the ‘receiving’ end of the cable to give the best termination at that end of the cable. The cable termination at Tx is essentially an open circuit when the bus line has been released and a short circuit when the bus is being driven LOW.

When Tx drives LOW the sending end of the cable is immediately driven near to 0 V and this 0 V propagates along the cable. After the propagation delay of the cable (approximately 5 ns/m) this causes the receiving end of the cable to be driven to 0 V. There will be some overshoot below 0 V because the termination is greater than the characteristic cable impedance. There will be reflected waves towards Tx and then back to the receiving end causing the received voltage to settle from below 0 V towards 0 V.

The overshoot below 0 V at the receiving end is applied to the Rx input of another P82B96 via a series 1 kΩ resistor with a clamping Schottky diode to ensure the level at Rx does not exceed its −0.5 V specification. Because the input current at Rx is always less than 1 μA there is negligible voltage drop on the 1 kΩ resistor so Rx receives a clean logic ‘LOW’ after just the one-way cable propagation delay. Raising the source impedance for any noise or ESD on the cable, using the 1 kΩ resistor, also makes it simple to provide ESD protection against large transient voltages using just a low power Zener fitted at the Rx terminal. The 18 V maximum rating at Rx means the Zener voltage is not critical and can be selected so the system is tolerant to large peak values above the nominal Zener rating. The junction diode in the Zener also provides protection for the small Schottky diode during large negative ESD transients.

When Tx releases the bus it is pulled HIGH by the 150 Ω pull-up at the ‘receiving’ end. The cable has been carrying a current approximately 4.6 V/150 Ω = 30.7 mA and this current continues to flow, causing Tx to rise by the product of this current and the characteristic impedance, so by about 3.1 V. This 3.1 V propagates to the receiving end and, after the propagation delay, causes a step in the voltage at the receiving end. That step level is calculated from the 3.1 V (appearing ahead of the cable characteristic impedance) and the 150 Ω pull-up to 5 V. The nominal level is
3.1 V + 1.9 × 100 / 250 = 3.86 V.

Because the 150 Ω termination is larger than the characteristic impedance, there will still be an exponential rise component in the waveform as it rises to that final value. The energy stored in the cable inductance is less than that needed to charge the cable capacitance and that extra energy must be supplied through the pull-up.

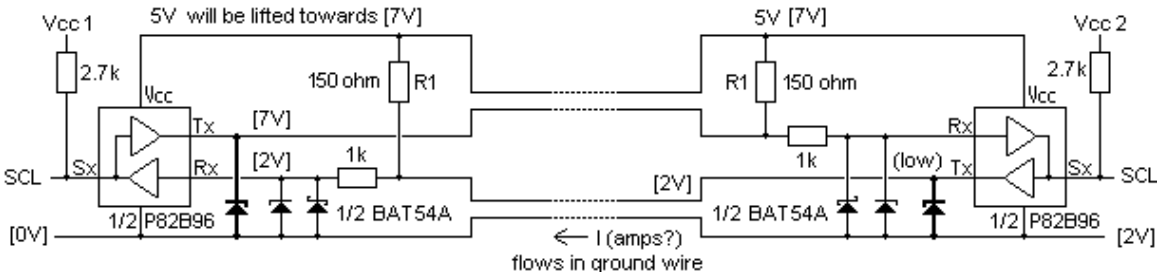
The logic threshold at Rx is V_{CC} / 2 = 2.5 V and a clean ‘HIGH’ level is achieved essentially after just a single cable propagation delay (again about 5 ns/m). The multiple reflections that cause subsequent level increases at the receiving end of the cable play no part in the timing.

Had a single transmission line been used then the first positive ‘step’ in the linked Tx/Rx signal at the ‘sending’ end, for a LOW-to-HIGH logic transition, would have been nominally 3.1 V. But that will have spreads, and ringing components, and could not be relied on to clear the 2.5 V Rx threshold. Should it fail to stay above 2.5 V on that first step, the next upward step of voltage will not occur until after **two** more cable propagations. For system timing calculation purposes the Rx level could not be guaranteed to be HIGH until after that extra time delay. For 100 m of cable, that would add an additional 1 μs of system delay, considerably slowing the maximum possible communication speed.

The 4-pair signaling approach eliminates timing uncertainty—and has other benefits as well. Some typical cable signal waveforms are shown in Section 4.4.1 and Section 4.4.2.

4.2 Handling ground potential differences

Figure 9 shows one example of the situation that must be handled when the ground potential at each end of the cable is different.



Right node sends 'LOW'.

Fig 9. Example of ground potential difference

In this example it is assumed that the node on the right hand side has a ground potential that is 2 V above the ground potential of the node on the left.

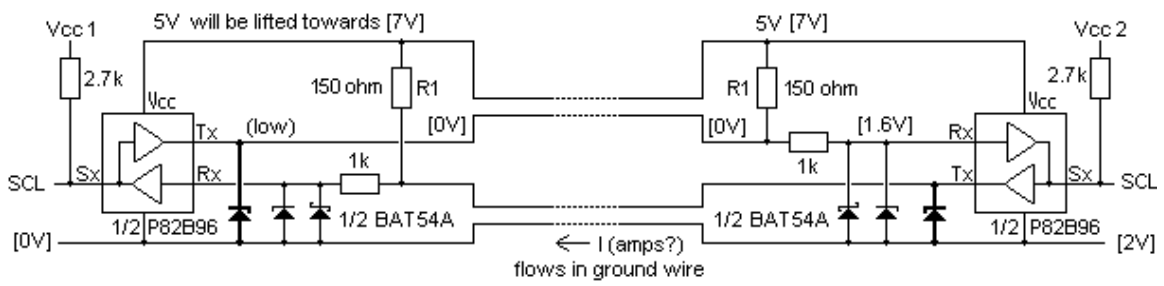
The numbers in brackets [n] show the voltages with reference to the ground on the left node.

The first point to note is that the ground potential difference will cause large currents to flow in the resistance of the cable ground leads. There will be at least two ground wires, only one half of the circuit is shown. The dc resistance of one ground lead is approximately 4.5 Ω/100 m so for two in parallel the resistance for 100 m is only 2.25 Ω.

If there really is a ground potential difference of 2 V, then there will be a current of almost 1 A flowing in the ground wires. Such currents are possible, for example, when equipment with large supply currents causes significant currents in the grounding system. Often any significant potential difference will therefore be an ac voltage, but it is easier to consider the cases with first a positive and then a negative difference.

When neither Tx is driven LOW, the voltages at all Tx/Rx pins are within their rating −0.5 V to +18 V and the level at both Rx pins is a valid 'HIGH' level.

Now firstly consider the case where the right hand node Tx pin transmits a 'LOW'. The Tx pin is then connected to its local ground and that has a potential of +2 V with respect to the node at the left. That 2 V is reproduced at the junction of the pull-up and 1 kΩ protection resistor connected to the Rx pin. It is not attenuated by that resistor and appears at the Rx pin. The Rx pin interprets any voltage < V_{CC} / 2 as low, so even with 2 V of ground difference the logic LOW signal will still be correctly received.



Left node sends 'LOW'.

Fig 10. Example of ground difference

Figure 10 shows the case for the left node transmitting a 'LOW'. In this case the Tx pin is pulled to 0 V relative to the left node's ground. That appears at the right hand node at the junction of the pull-up and protection resistors as 0 V. Because the right hand ground node is at +2 V, the Schottky diode at Rx will conduct and pull the Rx pin up to approximately 1.6 V. A harmless current of 1.6 mA will flow in the protection resistor. Relative to the local ground of the right hand P82B96 the Rx pin is at −0.4 V. That is within the chip's allowable voltage range (maximum −0.5 V) and represents a logic 'LOW', so again the logic level has been correctly transmitted even though there is significant ground difference.

Hopefully it is clear that because the arrangement is symmetrical it makes no difference which node is used as the 0 V reference. So if the right hand node was −2 V with respect to the left, that is simply the same case as when the left node is +2 V with respect to the right, and we have covered the case where one node is +2 V with respect to the other.

The only point to note is that in Figure 10, where the right hand node is more positive, the voltage applied to the Tx pin on the left is equal to the nominal supply plus the ground difference and the Tx pin has a data sheet rating of 18 V max. If this arrangement was used with 12 V supplies, that limits the ground difference to 6 V max and the practical working maximum might be around 5 V of ground difference.

Where the P82B96 V_{CC} is directly supplied via voltage regulators there is likelihood that one supply will be lifted above the nominal value. That causes no problems for P82B96 or signal transmission but if **other** devices, with lower V_{CC} ratings, are connected to the same supply then it may be necessary to insert some small series resistance in the P82B96 V_{CC} supply to prevent the supply regulator output being raised.

Whenever the ground potential differences are likely to cause unreasonable currents to flow in the cable ground wires it will be better to include true galvanic isolation using opto couplers or similar techniques.

4.3 Designing for extreme ESD requirements

While the P82B96 passes high ESD testing and is often used without any further protection, the introduction of very long cables opens the possibility for coupling of high energy transients during, for example, nearby lightning strikes or fault current interruption in ac mains distribution systems.

In these cases, the relatively low impedances of the communications cable bus allows the use of transient absorbing devices such as high power Zener diodes / transient suppressor diodes even though these devices feature quite high junction capacitance. The high voltage rating of the Tx pin allows the use of higher clamping voltages, and higher voltage Zeners will have lower capacitance.

Zeners or TVS diodes with a nominal voltage rating of, for instance, 10 V and pulse power ratings > 500 W fitted to Tx will generally be suitable when the cable supply is 5 V.

Because the 1 kΩ protection resistor limits the transients in the protection Zener at Rx it will usually be sufficient to use smaller surface mount Zeners there. When very high pulse ESD survival is required, the construction of the 1 kΩ resistor needs to be selected to survive the testing that will be applied to it.

In general, it becomes possible to select protection devices to pass any level of required tolerance to ESD.

4.4 Calculating timing delays and maximum data transmission speeds

To estimate the maximum I²C-bus clock speed that still guarantees the bus timing requirements are met, it is necessary to know:

- The minimum allowed clock HIGH and LOW periods for the ICs in the system
- The response times of the ICs, that is, the time taken for them to output valid acknowledge or data signals on SDA following their reception of a falling edge of the SCL signal
- The propagation delays of the SCL and SDA signals caused by the P82B96/PCA9600 and the cable
- The bus rise and fall times.

The timing requirement is that the ACK or data be valid on the SDA pin of the Master with the specified margin (set-up time) before the end of each SCL LOW period.

To calculate that, it is necessary to determine the times taken for the falling edge of the SCL master signal to reach the remote slave and the time taken for valid data on SDA to return to the master. The SDA signal may include significant delays due to slow rise times at the slave, so usually the critical delay will be calculated for a data ‘HIGH’ to become valid on the SDA pin of the master.

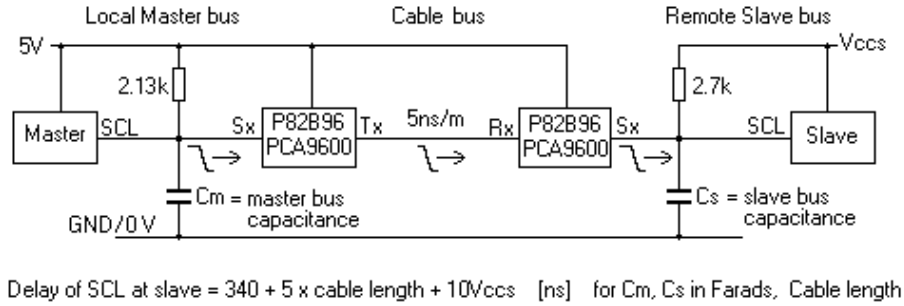


Fig 11. SCL as received at the slave is delayed (uses P82B96 delays)

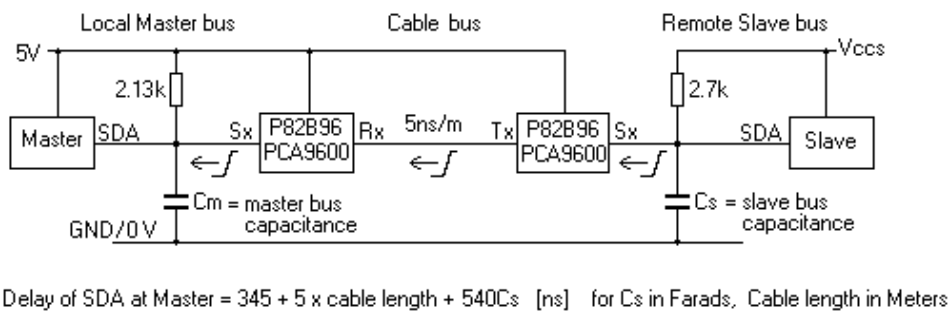


Fig 12. SDA signal received back at master is delayed (uses P82B96 delays)

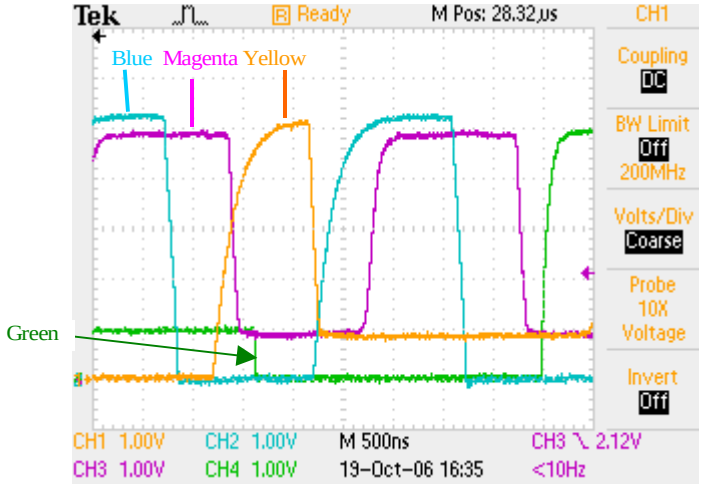
Figure 11 and Figure 12 show those two delays and how they may be approximated when the buffer used is P82B96.

On the SCL falling edge the delay components of P82B96 are the fixed delays Tx-to-Sx + Sx-to-Tx (total 255 ns) plus the fall time from 5 V to V_{IL} = 0.65 V at 20 ns/V (85 ns). At the slave, the approximation $10V_{CCS}$ for the SCL slave delay also assumes a typical 20 ns/V falling edge rate. It is the rate that would be achieved into a 120 pF load based on a dynamic sink capability of at least 6 mA— which all Fast-mode parts must have to meet the 300 ns fall time with a 400 pF load plus 3 mA resistive load.

The rise time components of SDA include the fixed delays of P82B96 (270 ns) plus the times for Sx at the master to rise from 0.8 V to 2.5 V, with the local capacitance of about 68 pF (75 ns), and for the slave SDA to rise from 0 V to 0.65 V, the switching level of Sx. The approximation quoted makes a compromise between 3.3 V or 5 V levels at V_{CCS}.

There is an Excel calculator which makes it easy to determine the maximum I²C-bus clock speed when using the P82B96 or PCA9600. The calculator and instructions can be found at www.nxp.com/clockspeedcalculator.

4.4.1 Example 1: Timings measured driving 50 m of cable between two P82B96s in 4-wire mode



Blue trace: SCL generated by the Master and applied at Sx of the P82B96 at the 'send' end of the cable.

Magenta trace: SCL signal as received at the PCA9633 slave at the remote end of the cable.

Green trace: SDA signal at the PCA9633 pin, at the remote end of the cable.

Yellow trace: SDA signal from PCA9633 as received from Sx back at the pin of the Master.

Fig 13. Driving PCA9633 at 350 kHz via a 50 m cable using P82B96 and 4-signal mode

Some of the important timing components are illustrated in Figure 13.

Firstly, the Master SCL signal as received by the PCA9633 slave has been delayed by about 620 ns by the cable and the two P82B96 buffers. The contributions (not shown here) are:

- the time for SCL to fall from 2.5 V (nominal logic threshold for the Master) to the 0.65 V switching threshold of Sx, about 50 ns
- propagation through P82B96 Sx to Tx at the Master end, including Tx fall time is 70 ns
- the cable propagation delay of approximately 5 ns/m or 250 ns
- the propagation from Rx to Sx at the slave end is 250 ns.

Total delay is 620 ns.

Next, the PCA9633 SDA provides an acknowledge of the received byte as shown by the green trace falling from the 0.8 V level output set by Sx to the near 0 V low driven by the PCA9633. The delay time to acknowledge is 200 ns. That represents the $t_{VD;ACK}$ delay or time to produce a valid ACK following the falling edge of the SCL that requests it.

The yellow trace shows that acknowledge signal as received back at the Master after the following delays:

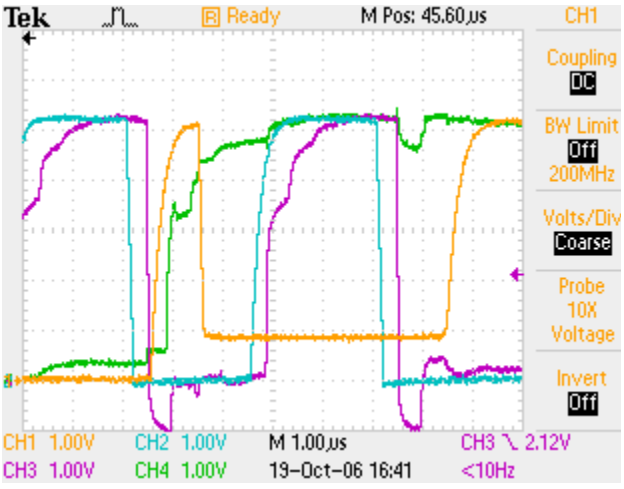
- the P82B96 propagation delay Sx to Tx of about 70 ns
- the cable propagation delay of 250 ns
- the propagation delay Rx to Sx at the master of 250 ns

for a total of 570 ns.

The yellow SDA signal becomes a valid ‘LOW’ just 100 ns before the master SCL crosses the logic threshold of about 2.5 V. That represents the limit timing situation for Fast-mode operation that requires the SDA to be valid 100 ns before the rising edge of the clock. It means that the SCL LOW period is the shortest one that still meets the Fast-mode microprocessor specified timing requirements.

In this example the SCL period time of 2860 ns (350 kHz) is approximately ‘LOW’ for 1520 ns and ‘HIGH’ for 1340 ns. If the micro allows programming an asymmetrical clock, the minimum HIGH period could be shortened to 600 ns and then full 400 kHz operation could be achieved while still meeting the other limit timings. Typical clock speed will be even higher.

To illustrate some of the other system waveforms, Figure 14 shows the ‘raw’ cable signals at Tx and at the end of the cable before the limiting action of the Schottky diode at Rx.



Blue trace: SCL drive signal at Sx of the P82B96 at the Master end.

Magenta trace: SCL measured directly on the cable, received at the slave end of the cable.

Green trace: SDA signal at Tx at the slave end of the cable.

Yellow trace: SDA at Sx at the slave showing the release of the ACK from near zero volts, rising to HIGH, but followed by the master driving SDA at Sx LOW again.The master’s SDA LOW at Sx is not returned to Tx, so the green trace stays HIGH.

Fig 14. Driving 50 m cable with P82B96 in 4-signal mode

Points to note include the reasonably controlled overshoot of the falling edge of SCL at the far end of the cable to about −1 V which would still exceed the rating of Rx if the series 1 kΩ and shunt Schottky diode had not been used. The effects of cross-coupling of the 4 signals and the voltage drop on the cable resistance also results in some distortions of

the waveforms, but always there is a reasonable safety margin between the signal level and the corresponding logic switching level. That represents the safety margin or noise margin available. The switching level at Rx is always very close to V_{CC} / 2, in this case 2.5 V.

4.4.2 Example 2: Shorter cable, 3 m, driven by P82B96 in 4-signal mode (for comparison with PCA9600 propagation delays)

Figure 15 shows the same waveforms as in Figure 13 above.

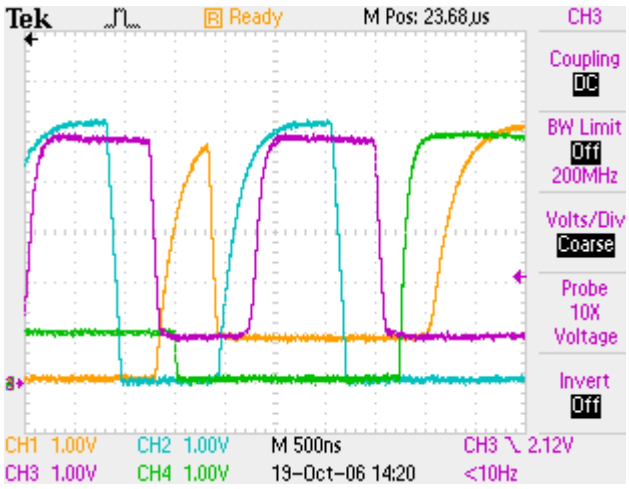


Fig 15. Waveforms with P82B96 driving 3 m cable in 4-signal mode

In this case the only decreased delay is the cable propagation delay, down from 250 ns to nominal 15 ns, but now too small to resolve accurately.

In theory, the SCL LOW period can only be decreased by 235 ns. That means decreased from 1520 ns for the 50 m cable to about 1285 ns. Here it is about 1150 ns, and still providing > 100 ns SDA set-up time, but the SDA example in the yellow trace in Figure 15 has a faster falling edge. The clock cycle in Figure 15 is 2275 ns or 440 kHz. Always remember that the 'typical' speeds are usually faster than the 'worst case' timing that we use for calculations.

PCA9600 reduces the IC propagation times to around 75 ns, saving about 350 ns and permitting a 'LOW' period of around 800 ns. With an Fm+ HIGH period of 260 ns and a reduced set-up time of 50 ns, it can achieve a cycle time around 1010 ns or 990 kHz on short cables.

For short cables there can be an advantage in using the 2-signal mode because the short cable adds negligible delays even if some reflections occur. Eliminating the second PCA9600 propagation delay by feeding the cable signal directly to an Fm+ slave ensures 1 MHz operation when using short cables, but always remember the margin that allows introducing any buffer or cable propagation delay is simply the timing margin between the measured or 'typical' response time to valid data of the slave (200 ns for PCA9633) and the Fm+ allowable limit delay of 450 ns. That difference, 250 ns, is significantly larger than the one-way PCA9600 propagation delays of about 75 ns so 1 MHz is possible when using one PCA9600 with reasonable cable delays.

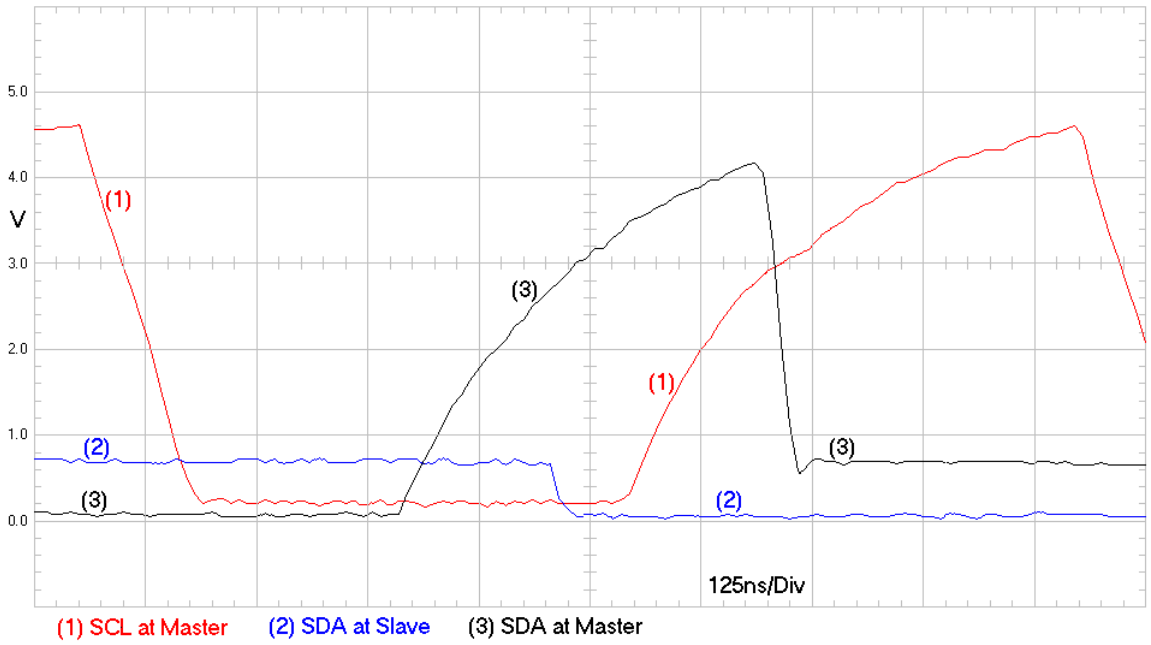


Fig 16. PCA9600 driving Fm+ slave over 20 m cable in 4-signal mode

Figure 16 shows a 1 MHz clock (1) as generated at the master. The Acknowledge by a PCA9633 slave (measured at the slave SDA pin) is shown (2) and the SDA waveform as measured at the master SDA pin is shown as (3).

In this example the black curve (3) shows firstly the master releasing the bus LOW after the 8th or Write bit approximately 300 ns after SCL goes LOW. That clock LOW propagates to the slave and the slave's Acknowledge response is shown by the blue trace (2) falling from the 0.7 V level to near zero. The 0.7 V level was the master Write bit and the master release has not propagated to the slave before the slave acknowledges so the temporary HIGH as seen at the master is not seen here. The slave's acknowledge propagates back to the master causing the SDA to fall to 0.7 V as shown in (3).

The total delay measured from the master clock going LOW until the slaves acknowledge reaches the master is approximately 700 ns. In this example the 1 MHz master clock has already gone HIGH before receiving the slave's acknowledge so this transmission will not succeed. The clock LOW period must be increased until the ACK is received with the required 50 ns set-up margin, meaning the SCL LOW must be longer than 750 ns. The maximum clock speed allowed in this example (20 meters/4-signal mode) will be about 800 kHz.

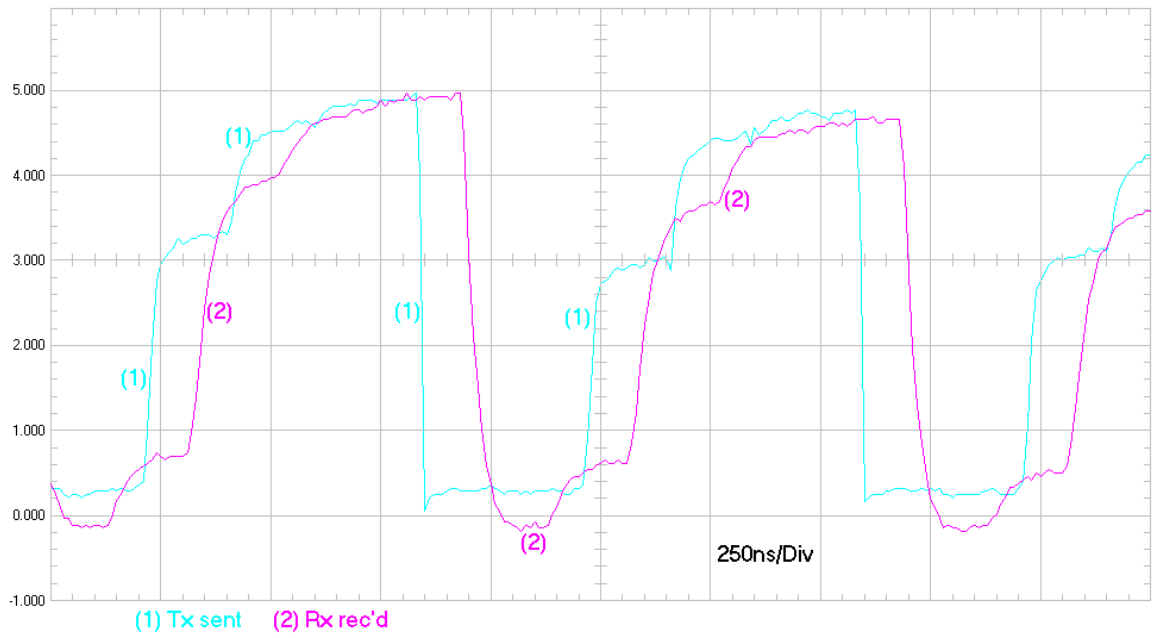
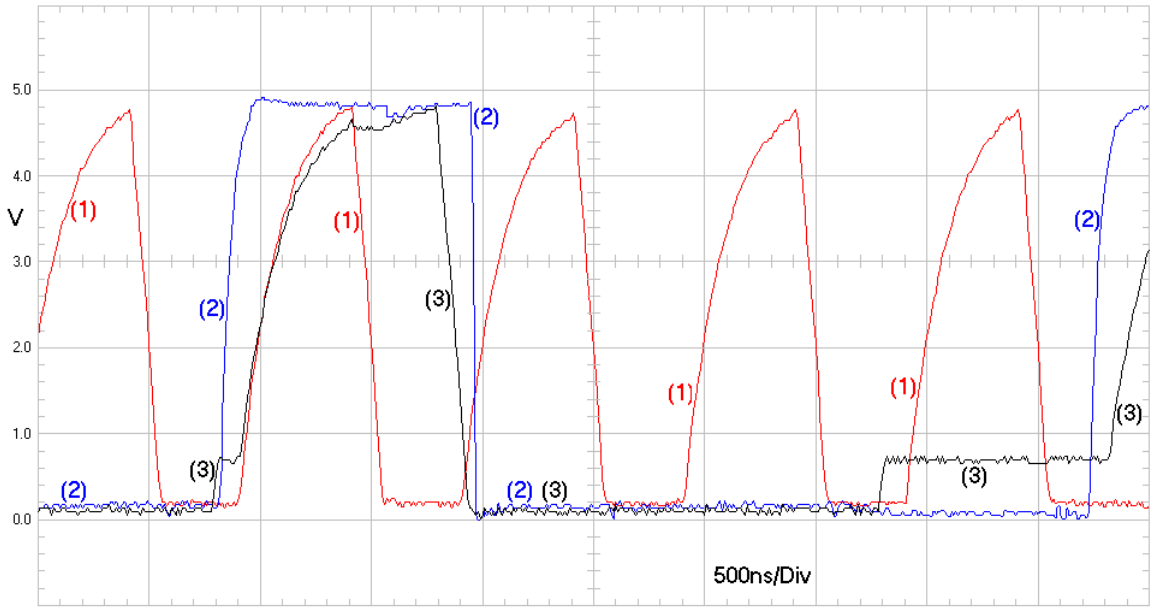


Fig 17. 1 MHz sends and receives signals on 20 m cable using PCA9600

Figure 17 shows the PCA9600 cable waveforms for comparison with P82B96 shown in Figure 7 in Section 3.2.

Because the Tx driver stage is very similar the difference is mostly the reduced cable delay. As before, the rising signal at Rx (2) is crossing the Rx threshold monotonically after the 100 ns cable delay, and ringing after the received falling edge is small.



(1) SCL at master micro pin

(2) Data at PCA9633 pin

(3) Data at master micro pin.

Fig 18. 1 MHz signals PCA9600 generating Fm+ signals and directly driving PCA9633

Figure 18 shows the timings for PCA9600 driven by 1 MHz signals from the I2C2005-1 evaluation board.

Switch 1 on the daughter board has been opened to avoid clock stretching because the Master micro on the evaluation board is not intended for 1 MHz operation. Switch 2 is closed as usual for normal bidirectional SDA signals.

Again, the Master timing is being pushed beyond its rated operation and the black trace (3) following the first and second falling clock edges from the left shows the t_{VD} for the micro generating address data bits is around 400 ns, leaving almost no margin for buffer delays. The 4th falling clock edge from the left is the start of the 9th clock, requesting acknowledge by the PCA9633 slave, and the ACK is returned to the master (see 0.7 V level at Sy) well before the clock goes HIGH and inside the t_{VD} of the master.

With signals from a master that is specified for Fm+ operation there will be even larger margins to ensure 1 MHz operation. As always, the buffer delays are accommodated by the safety margins of the Fm+ devices and unless those margins are specified in their t_{VD} ratings the designer should slow the clock to accommodate the buffer delays.

4.5 Alternative components for ESD protection

As described in Section 4.3, provision is made for fitting of ESD protection components to achieve very high levels of immunity when this is a requirement.

Diodes D1, D4 can be large axial or SMD protection diodes to provide for the Tx pin. They should be chosen to clamp the peak voltage at Tx to the maximum rating (18 V) of this pin when the required test pulses are applied to the cable. Diodes D2, D5 can be smaller SMD Zener diodes from the BZX84-Cxx or similar families.

4.6 P82B96/PCA9600 evaluation board, PCB artwork and bill of materials

The PCB layout and bill of materials are given in Figure 19 and Table 1.

Table 1. Bill of materials

Part type	Designator	Footprint	Description
2.54 mm 4×2 way header	J2	4×2 way 2.54 mm PIN HEADER	Test point connector
Molex 22-28-6270	CON4	9 way 2.54 mm PIN HEADER	9-pin connector
Molex 22-15-2096	CON3	9 way 2.54 mm PIN SOCKET	9-pin socket
	R8	R0805	SMD resistor
	R4	R0805	SMD resistor
Multicomp 7005-8P8C	CON2	RJ-45 8TH	RJ-45 8 way connector
Multicomp 7005-8P8C	CON1	RJ-45 8TH	RJ-45 8 way connector
1 kΩ	R10	R0805	SMD resistor
1 kΩ	R6	R0805	SMD resistor
2.7 kΩ	R1	R0805	SMD resistor
2.7 kΩ	R2	R0805	SMD resistor
100 nF	C1	C0805	SMD capacitor
150R	R9	R0805	SMD resistor
150R	R5	R0805	SMD resistor
	R7	AXIAL VR25(0.4)	user installed leaded resistor
	R3	AXIAL VR25(0.4)	user installed leaded resistor
	D1	DIODE SOD57 (0.5)	user installed leaded Zener diode
	D4	DIODE SOD57 (0.5)	user installed leaded Zener diode
BAT54A	D3A	SOT23	Schottky diode
BAT54A	D3B	SOT23	Schottky diode
BZX84C15	D5	SOT23	user installed SMD Zener diode
BZX84C15	D2	SOT23	user installed SMD Zener diode
2.54 mm 3 way header	J1	3 way 2.54 mm PIN STRIP	supply selector header
P82B96	IC1	SO8	dual bidirectional bus buffer
OMRON A6T-4104	S1	DIP8	DIP switch

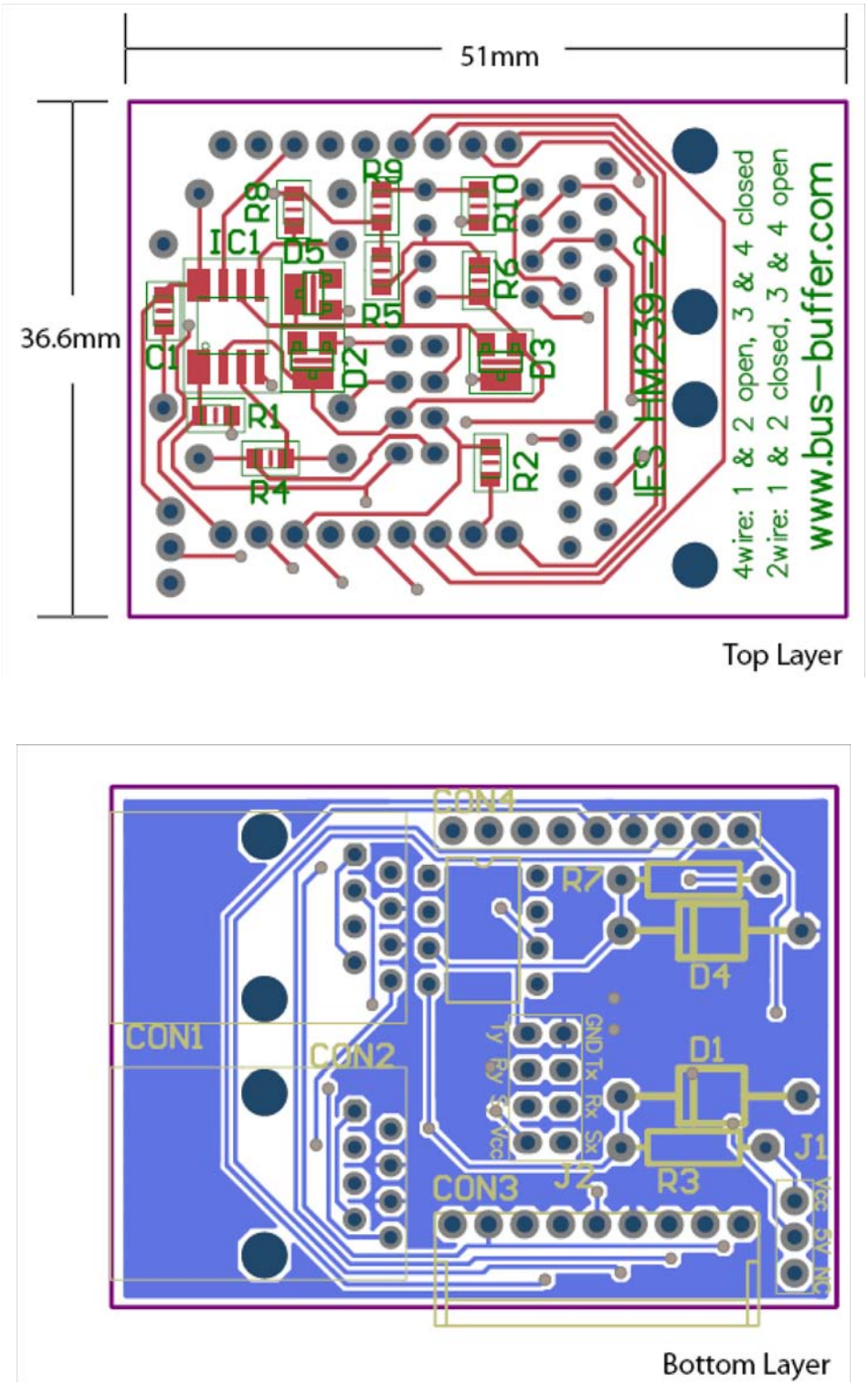


Fig 19. PCB layout

5. Development tools available from NXP Semiconductors

Refer to the **Tools** section of the NXP I²C-bus web site: www.nxp.com/products/interface_control/i2c/tools/

6. Support literature

Refer to **Support** section of the NXP I²C-bus web site: www.nxp.com/i2c/support/

7. Abbreviations

Table 2. Abbreviations

Acronym	Description
DIP	Dual In-line Package
DVD	Digital Versatile Disc
ESD	ElectroStatic Discharge
Fm+	Fast-mode Plus
I²C-bus	Inter-IC bus
I/O	Input/Output
IC	Integrated Circuit
LED	Light Emitting Diode
PCB	Printed-Circuit Board
SMD	Surface Mounted Device
STB	Set-Top Box
TTL	Transistor-Transistor Logic
TVS	Transient Voltage Suppressors
USB	Universal Serial Bus

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9. Contents

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